REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-23 in the application. In a previous response, the Applicant amended Claims 4, 12 and 20 to correct informalities. In the present response, no claims have been amended, canceled or added. Accordingly, Claims 1-23 are currently pending in the application.

I. Rejection of Claims 1-23 under 35 U.S.C. §102

The Examiner has rejected Claims 1-23 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,832,292 to Nguyen, *et al.* (Nguyen). The Applicant respectfully disagrees since Nguyen does not teach reducing pipeline stalls between nested calls including storing return PC values in return PC storage located in an execution core of a processor and making ones of the return PC values available to a PC of the processor upon execution of corresponding return instructions as recited in independent Claims 1, 9 and 17.

Nguyen teaches a microprocessor having an Instruction Execution Unit (IEU) 104 and an Instruction Fetch Unit (IFU) 102 that includes a Program Counter (PC) logic unit 270. (*See* column 6, lines 60-63, column 8, lines 42-43, column 12, lines 38-41, and Figures 1-3.) The PC logic unit 270 includes a prefetch PC control unit 364 and an execution PC control unit 366 that provides an address for prefetching. (*See* column 16, lines 43-46, column 17, lines 14-16 and Figure 3.) The prefetch address provides a return address for subsequent use by the prefetch PC control unit 364 when an initial call, trap or procedural instruction occurs. The prefetch address is stored in registers in the prefetch PC control unit 364 upon each occurrence of these instructions. (*See* column 17, lines 16-19.)

Nguyen does not teach, however, making the prefetch addresses available upon execution of corresponding return instructions. On the contrary, Nguyen teaches selecting one of the return address registers in the prefetch PC control unit 364 to provide a new prefetch virtual address after